Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A serial line circuit comprising:

a bus;

a plurality of isolators interposed between two portions of the bus;

a first component coupled to the bus, the first ~~programmable~~ component to transfer information via a first isolator of the plurality of isolators; and

a second component coupled to the bus, the second component to transfer sampled information over the bus via a second isolator of the plurality of isolators, the second isolator being different from the first isolator.

2. (original) The serial line circuit of claim 1, wherein the plurality of isolators is a pair of isolators including the first isolator and the second isolator.

3. (currently amended) ~~The~~ A serial line circuit comprising: ~~of claim 1~~

a bus;

a plurality of isolators interposed between two portions of the bus;

a first component coupled to the bus, the first component to transfer information via a first isolator of the plurality of isolators, ~~wherein~~ the first component is a programmable component being a field programmable gate array (FPGA) to multiplex serial data ~~received from a plurality of serial Universal Asynchronous Receiver Transmitters (UARTs)~~ and to transfer the serial data over the bus via the first isolator; and

a second component coupled to the bus, the second component to transfer sampled information over the bus via a second isolator of the plurality of isolators.

4. (original) The serial line circuit of claim 3, wherein the second component is a programmable component being a complex programmable logic device (CPLD) that samples data from a plurality of serial connectors and routes the sampled data over the bus via the second isolator.

5. (currently amended) ~~The~~ A serial line circuit comprising: ~~of claim 1~~

a bus;

a plurality of isolators interposed between two portions of the bus;

a first component coupled to the bus, the first component to transfer information via a first isolator of the plurality of isolators; and

a second component coupled to the bus, the second component to transfer sampled information over the bus via a second isolator of the plurality of isolators, ~~wherein~~ the first component to receive serial data bits, multiplex the received serial data bits by forming data frames each including a plurality of overhead bits along with a serial bit of the received serial data bits, and to transfer the overhead bits along with the serial bit to the second component over the bus via the first isolator, the overhead bits including a serial port number to identify a serial line connector to receive the serial bit corresponding to the overhead bits.

6. (original) The serial line circuit of claim 5, wherein the first component receives the serial data bits from a plurality of serial Universal Asynchronous Receiver Transmitters (UARTs).

7. (cancelled)

8. (currently amended) The serial line circuit of claim [[7]] 5, wherein the overhead bits include a valid bit to identify whether the serial bit is valid.

9. (currently amended) The serial line circuit of claim [[7]] 5, wherein the second component to receive a first data frame and to transfer a serial bit of the first data frame to a serial line connector determined by the serial port number contained in the overhead bits.

10. (currently amended) An electronic device comprising:

a plurality of serial port connectors; and

a serial line circuit coupled to the plurality of serial port connectors, the serial line circuit comprises

a first programmable component,

a second programmable component in communication with the plurality of serial port connectors,

a bus coupled to the first programmable component and the second programmable component,

a first isolator situated along the bus, the first isolator to receive a serial data bit preceded by control information from the first programmable component for transfer to the second programmable component, and

a second isolator situated along the bus, the second isolator to ~~receiver~~ receive a sampled data bit preceded by control information from the second programmable component for transfer to the first programmable component.

11. (original) The electronic device of claim 10, wherein the first programmable component of the serial line circuit comprises a field programmable gate array (FPGA) to multiplex serial data received from a plurality of serial Universal Asynchronous Receiver Transmitters (UARTs) and to transfer at least the control information and the serial data bit of the serial data over the bus via the first isolator.

12. (original) The electronic device of claim 11, wherein the second programmable component of the serial line circuit comprises a complex programmable logic device (CPLD) that samples data from the plurality of serial port connectors and routes the sampled data over the bus via the second isolator.

13. (original) The electronic device of claim 10, wherein the first programmable component of the serial line circuit to receive serial data bits including the serial data bit, to multiplex the received serial data bits by forming data frames, one of the data frames including a serial port number along with the serial data bit, and to transfer the serial port number along with the serial data bit to the second programmable component over the bus via the first isolator.

14. (original) The electronic device of claim 13, wherein the one of the data frames formed by the first programmable component further comprises a valid bit to identify whether the serial data bit is valid.

15. (currently amended) The electronic device of claim [[10]] 13, wherein the second programmable component to receive one of the data frames and to transfer the serial data bit to a first serial port connector of the plurality of serial port connectors determined by the serial port number.

16. (currently amended) A method comprising:

receiving a plurality of serial data bits;

multiplexing the plurality of serial data bits in order to transfer the serial data bits over an interconnect through a single isolator, the multiplexing comprises generating control information for each serial data bit of the plurality of data bits and transferring the control information along with a corresponding serial data bit immediately after each other, and a transmission rate of the interconnect exceeds a transmission rate of at least one interconnect providing the corresponding serial data bit by a factor of at least one-hundred; ~~and~~

recovering each of the plurality of serial data bits; and

determining a serial port connector for each of the plurality of serial data bits for routing to the serial port connector.

17-18. (cancelled)

19. (currently amended) The method of claim [[18]] 16, wherein the control information comprises a serial port number.

20. (original) The method of claim 19, wherein the control information further comprises a valid bit to identify whether the corresponding serial data bit is valid.